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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

MARTINEZ, DAVID E

ART UNIT	PAPER NUMBER
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2182

DATE MAILED: 08/20/2003

8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/928,797

Applicant(s)

NIE ET AL.

Examiner

David E Martinez

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 August 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 8/13/01 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Drawings

Figure 2 is objected to because it is missing element reference numerals. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "the ROM memory" in claim 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitter Prior Art (hereinafter referred to as "AAPA") in view of US Patent No. 5,706,466 to Dockser.

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In regards to claim 1, AAPA teaches a high speed processor (fig 2) having:
a data processing unit for processing data (fig 2, element labeled "data processing unit" page 2 lines 20,21) ;

a data memory (fig 2, element labeled "data memory") which is connected to the data processing unit (fig 2, element labeled "data processing unit") via a data bus (fig 2, element labeled "data bus");

at least one input interface buffer (fig 2, element labeled "port in") which is connected to the data bus (fig 2, element labeled "data bus")

and has the purpose of buffering input data (page 2 lines 9,10);

at least one output interface buffer (fig 2, element labeled "port out", page 2 lines 24-29) which is connected to the data bus (fig 2, element labeled "data bus")

and has the purpose of buffering output data (page 2 lines 24-29);

the input interface buffer and the output interface buffer being directly

addressable by the data processing unit via an interface address bus.

The AAPA teaches all that is claimed above, the data memory and input and output ports all connected to the same address bus, communicating with the data processing unit. AAPA does not disclose the data memory having its own "data memory address bus" to the data processing unit. The AAPA also fails to disclose the input and output interface buffers having their own "interface address bus" connected to the data processing unit.

Dockser teaches no matter how fast the processor, performance cannot be increased once the bandwidth of a bus is fully used. The use of separate buses doubles the communication bandwidth in a system (column 2, lines 25-57).

It would have been obvious to one of ordinary skill in the art at the time of the invention to separate the "address bus" disclosed in the AAPA into two buses, the "data memory address bus" and the "interface address bus" because it increases performance and doubles the bandwidth in the system.

In regards to claim 2, AAPA teaches a high speed processor (fig 2), wherein the data memory (fig 2, element labeled "data memory") contains at least one RAM memory (fig 2, elements labeled "RAM" page 2, lines 15,16).

In regards to claim 3, AAPA teaches a high speed process, wherein the data processing unit (fig 2, element labeled "data processing unit") is connected to the ROM memory (fig 2, element labeled "ROM") which stores program data (page 2, lines 22-24).

In regards to claim 4, AAPA teaches a high speed processor (fig 2), wherein the data processing unit (fig 2, element labeled "data processing unit") is an RISC data processing unit (page 2 lines 30-35).

In regards to claim 5, AAPA teaches a high speed processor (fig 2), wherein the data processing unit (fig 2, element labeled "data processing unit") contains a plurality of addressable internal registers (fig 2, element labeled "R" page 2 lines 20,21).

In regards to claim 6, AAPA teaches a high speed processor (fig 2), wherein

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the data processing unit (fig 2, element labeled "data processing unit") can carry out a plurality of data transfer processor commands in order to directly exchange data between the data memory (fig 2, element labeled "data memory"), the registers (fig 2, element labeled "R") and the interface buffers (fig 2, elements labeled "port in" and "port out")(examples on page 4, lines 9-31).

In regards to claim 7-11, 21, AAPA teaches a high speed processor (fig 2), wherein a data transfer processor command is carried out by the data processing unit. The data is loaded from source to target locations. AAPA teaches examples of this on page 4, lines 9-31.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teaching from the AAPA to process data transfer commands from one memory source to another. Memory storage locations are arbitrary and the differences in data transfer commands are dependent only on address specification.

In regards to claim 12, AAPA teaches a high speed processor (fig 2), wherein the input interface buffer (fig 2, element labeled "port in" is connected to an analog/digital converter (fig 2, element labeled "A/D", page 2 lines 6-10).

In regards to claim 13, AAPA teaches a high speed processor (fig 2), wherein the output interface buffer (fig 2, element labeled "port out") is connected to a D/A converter (fig 2, element labeled "D/A", page 2 lines 24-28).

In regards to claim 14, it is inherent the data ' processing unit connects to both input and output interface buffers via control lines.

In regards to claim 15, AAPA teaches a high speed processor (fig 1 is a black box diagram of fig 2), wherein the input interface buffer is an, xDSL interface buffer for buffering xDSL data (page 1, lines 13-29).

In regards to claim 16, AAPA teaches a high speed processor as claimed in claim 15, wherein the xDSL input interface buffer has a data frame detecting device for detecting a data frame synchronization data pattern (while the AAPA may not explicitly teach this, it discloses that it processes predefined data format, page 1 lines 22-32).

In regards to claim 20, it is well known in the art wherein processor internal registers have a plurality of memory locations for different data words.

In regards to claim 22, AAPA teaches a high speed processor (fig 2), wherein peripherals can be connected to the interface buffers (page 2 lines 6-9, 24-29). "DQ" and "data sink such as a terminal" are examples taught by the AAPA as peripherals.

In regards to claim 23, it is well known in the art to have configurable communication ports.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitter Prior Art (hereinafter referred to as "AAPA") in view of US Patent No. 5,706,466 to Dockser in further view of US Patent No 5,400,369 to Ikemura.

In regards to claims 17, 18, AAPA discloses the high speed processor having a data frame detecting device (can recognize data formats, page 1, lines 22-32) but fails to explicitly disclose the details about the data frame detecting device of claim 16 above.

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Ikemura discloses a data frame detecting device having a shift register (fig 2, element 101, column 3 lines 1-5) for writing in input data, a data pattern memory (fig 2, element 102, column 3 lines 5-15) for storing the data frame synchronization data pattern and a comparator (fig 2 element 102, column 3 lines 5-15) device for bit-by-bit data comparison of the input data written into the shift register, and of the data frame synchronization data pattern stored in the data pattern memory, the comparator device generating a data frame detection signal (column 3, lines 15-20) if the input data written into the shift register is identical to the stored data frame synchronization data pattern;

after the data frame detection signal generated, the shift register is expanded to form a toroidal memory for buffering data (column 6 lines 35-61).

Ikemura discloses the above data frame detecting device to reduce the size of byte and frame alignment circuitry and also to increase the operating speed of byte and frame alignment circuitry (column 1, lines 55-60).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the teachings of ikemura to the applicants invention in order to reduce the size of the circuitry and increase the operating speed.

In regards to claim 19, it is well known in the art to output modulated data such as PCM data through a medium. It would have been obvious to have the output interface buffer be a PCM interface buffer for buffering PCM data.

Conclusion

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The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E Martinez whose telephone number is (703) 305-4890. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DEM


KIM HUYNH
PRIMARY EXAMINER 8/19/03